Tishk International University
Science Faculty
IT Department

Computer Hardware

Lecture 02: CPU

2nd Grade – Fall Semester

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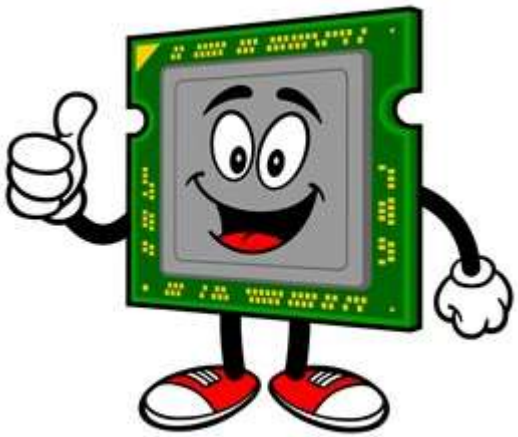
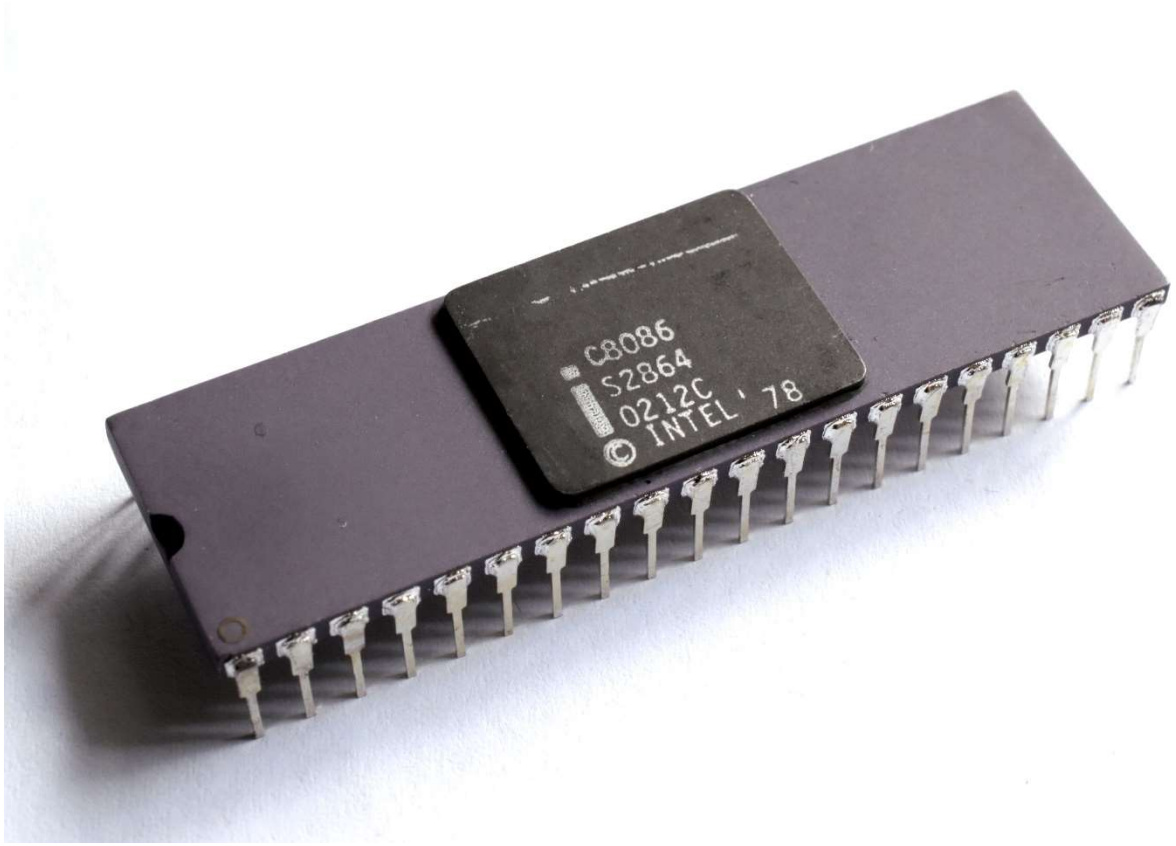
Lecture 2- CPU

	Topic
Part 1	**Intel 8086**
Part 2	**Intel 80386**
Part 3	**Intel CPU Evolutions**



Lecture 02: CPU
PART1- Intel 8086



8086/8088 Features

- IBM PC was based on Intel 8088 CPU.
- Intel has manufactured two 16-bit CPUs
  - 8086 has 16-bit registers with 16-bit external data bus.
  - 8088 has 16-bit registers with 8-bit external data bus.
- 8086/8088 has a 20 bit address bus which can address up to 2^{20} memory locations then we can write:

$2^{20} = 2^{10} * 2^{10} = 1K * 1K = 1$ MB

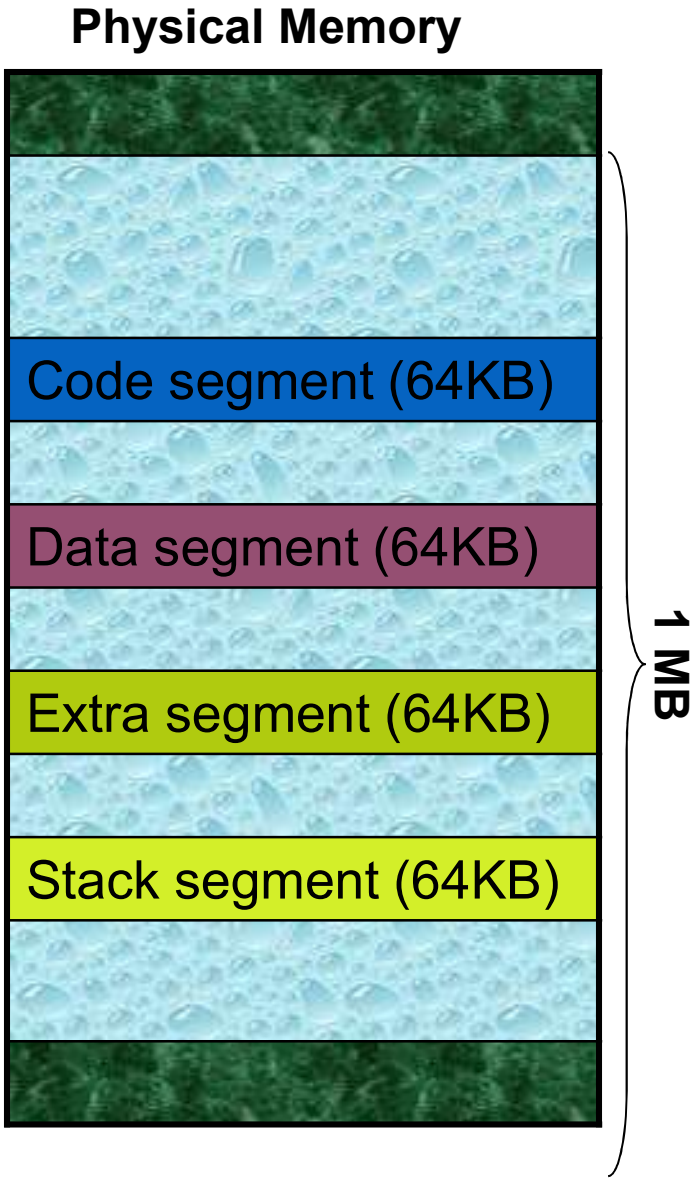
- So the maximum physical memory is (1 MB)
- Address ranges from 00000H to FFFFFH and Every byte has a separate address.
- The memory in an 8086 based system is organized as segmented memory.

Segmented Memory

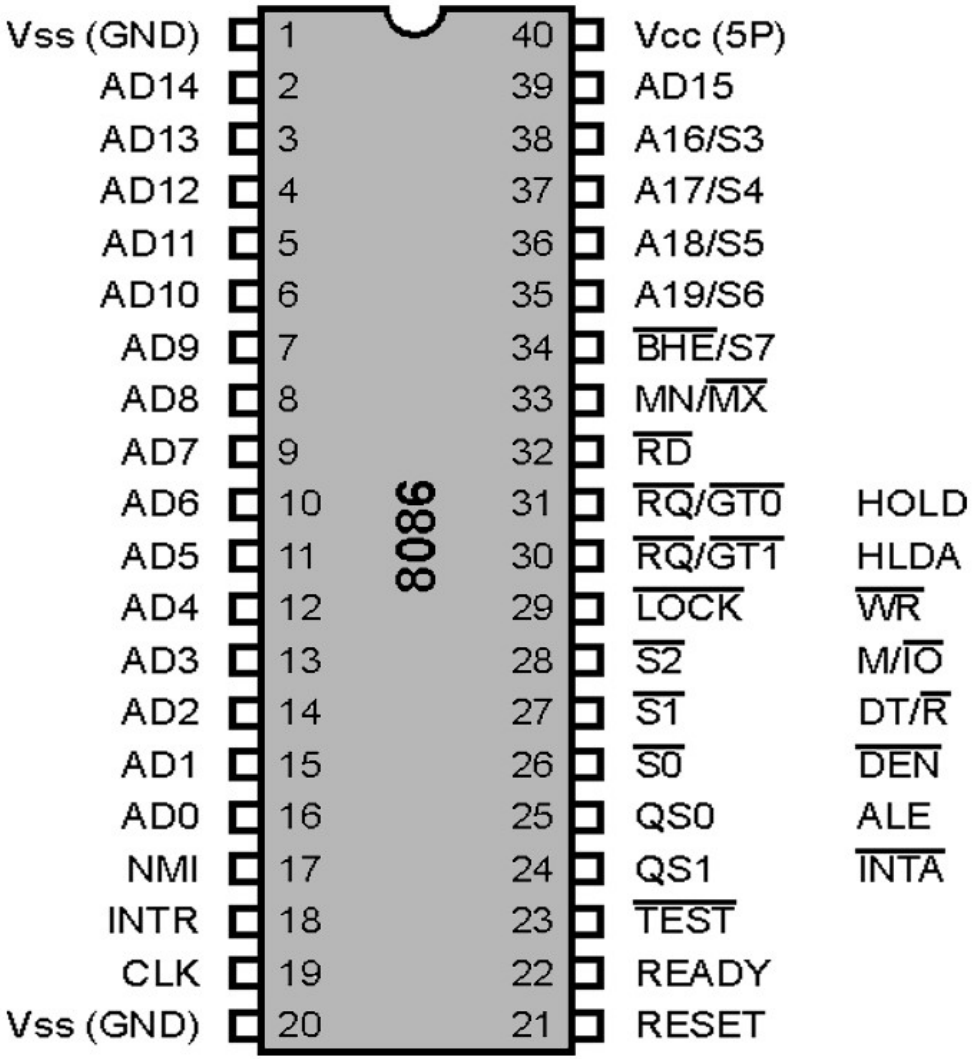
- In 8086 physically memory is divided into a number of logical segments.
- the processors have 4 segments registers, and all are 16 bit registers, each register refers to start of a segment:
  - Code Segment register (CS),
  - Data Segment register (DS),
  - Extra Segment register (ES) and
  - Stack Segment register (SS).

Advantages of Segmented memory Scheme

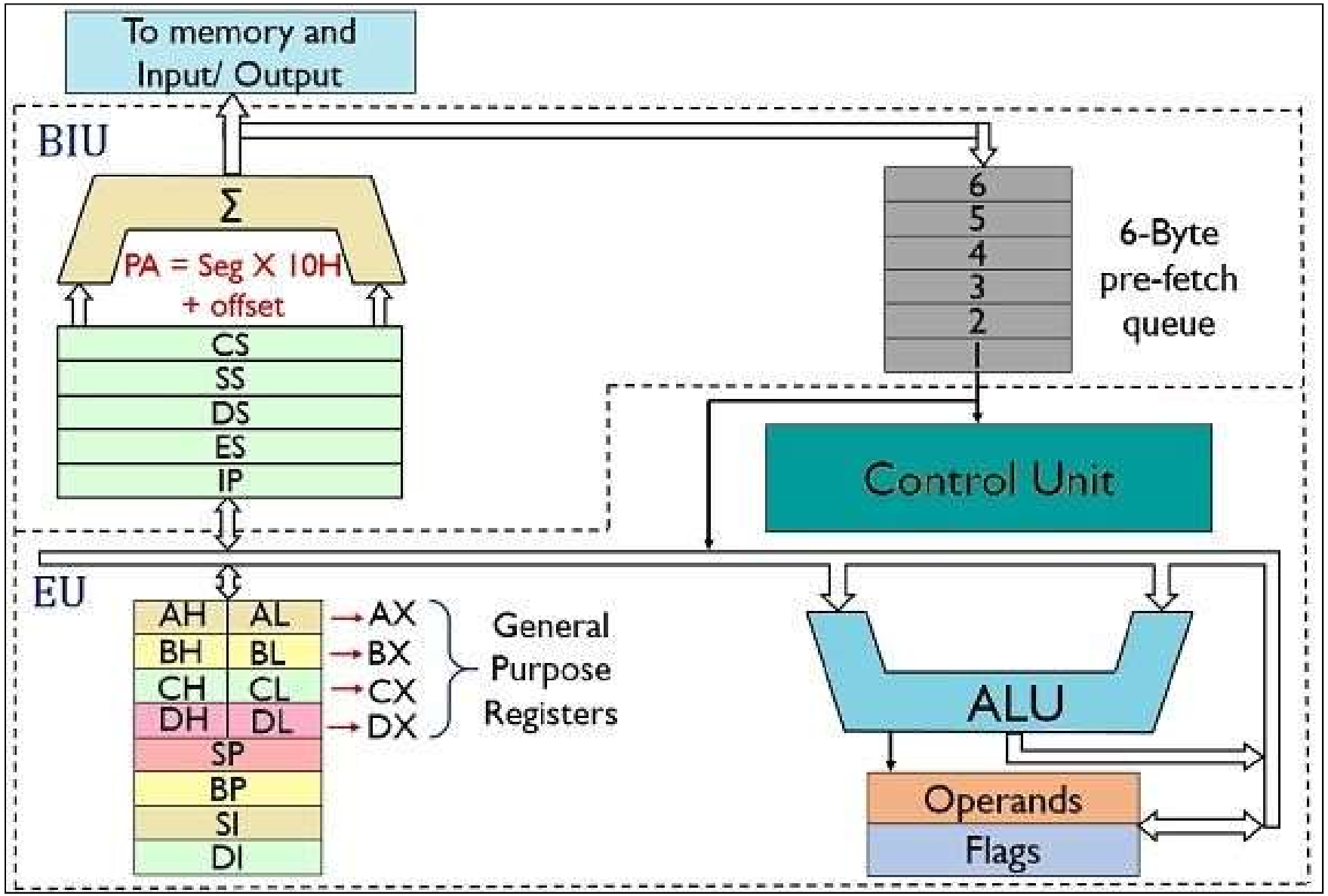
- Allows the placing of code, data and stack portions of the same program in different parts of the memory.
- Permits code and data to be put into different areas of memory each time program is executed.



Intel 8086 Pinout
(not required in the exam)



Block Diagram of Intel 8086 Architecture



Internal architecture of 8086

- **8086 has two blocks**
  - **Bus Interface Unit (BIU)**
  - **Execution Unit (EU).**

- **Both units operate asynchronously to give the 8086 an overlapping instruction fetch and execution mechanism which is called as Pipelining. This results in efficient use of the system bus and system performance.**

BUS INTERFACE UNIT (BIU)

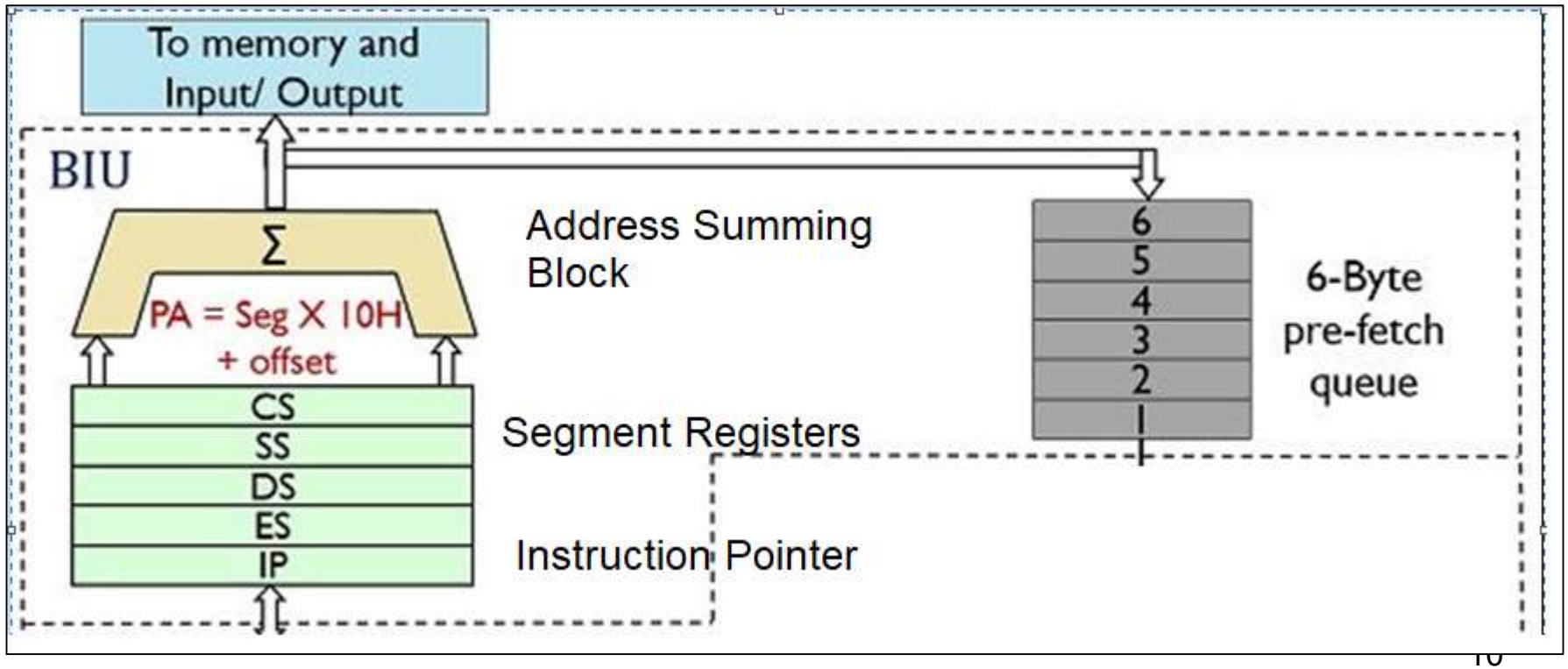
The BIU performs below operations:

- instruction fetching,
- storing instruction in pre-fetch queue.
- reading and writing operands for memory and
- calculating the addresses of the memory operands.

BUS INTERFACE UNIT (BIU)

BIU Contains:

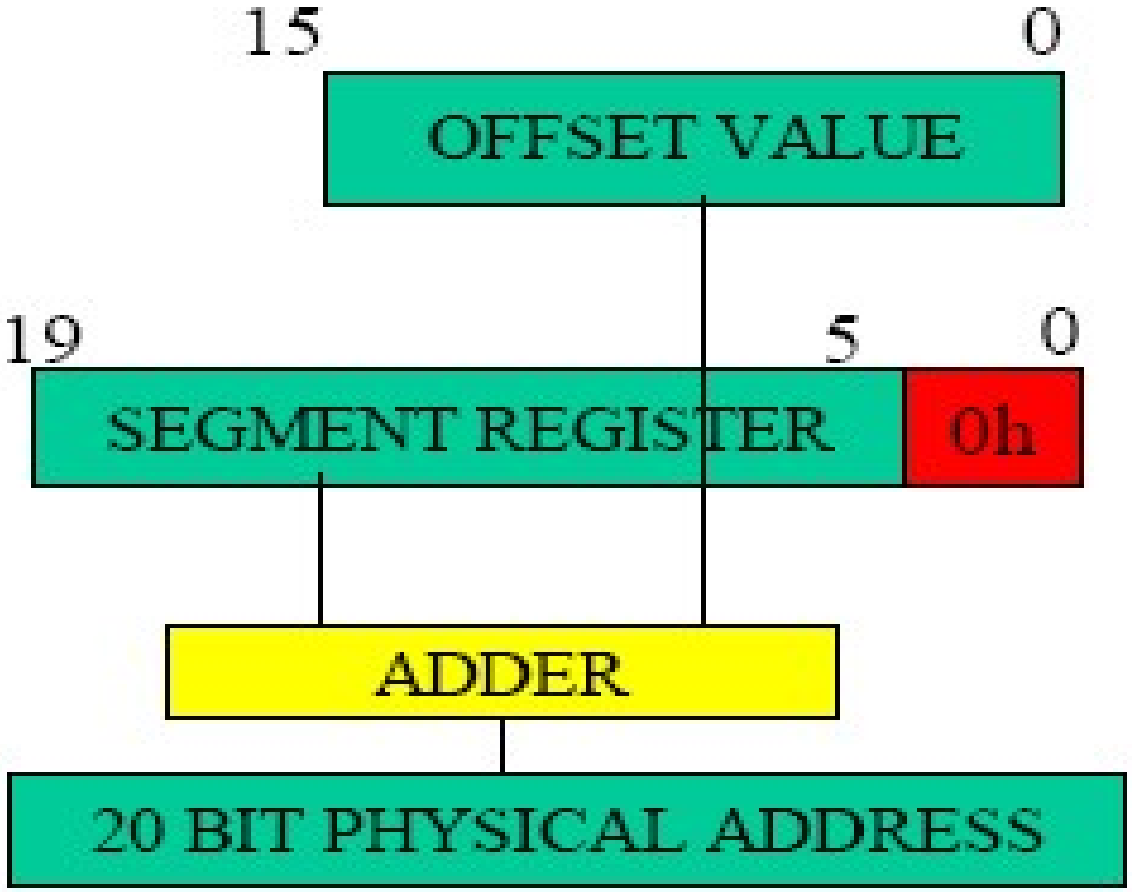
- **Pre-fetch Queue**
- **The Segment Registers (CS, DS, ES, SS).**
- **The Instruction Pointer (IP).**
- **The Address Summing block (Σ)**



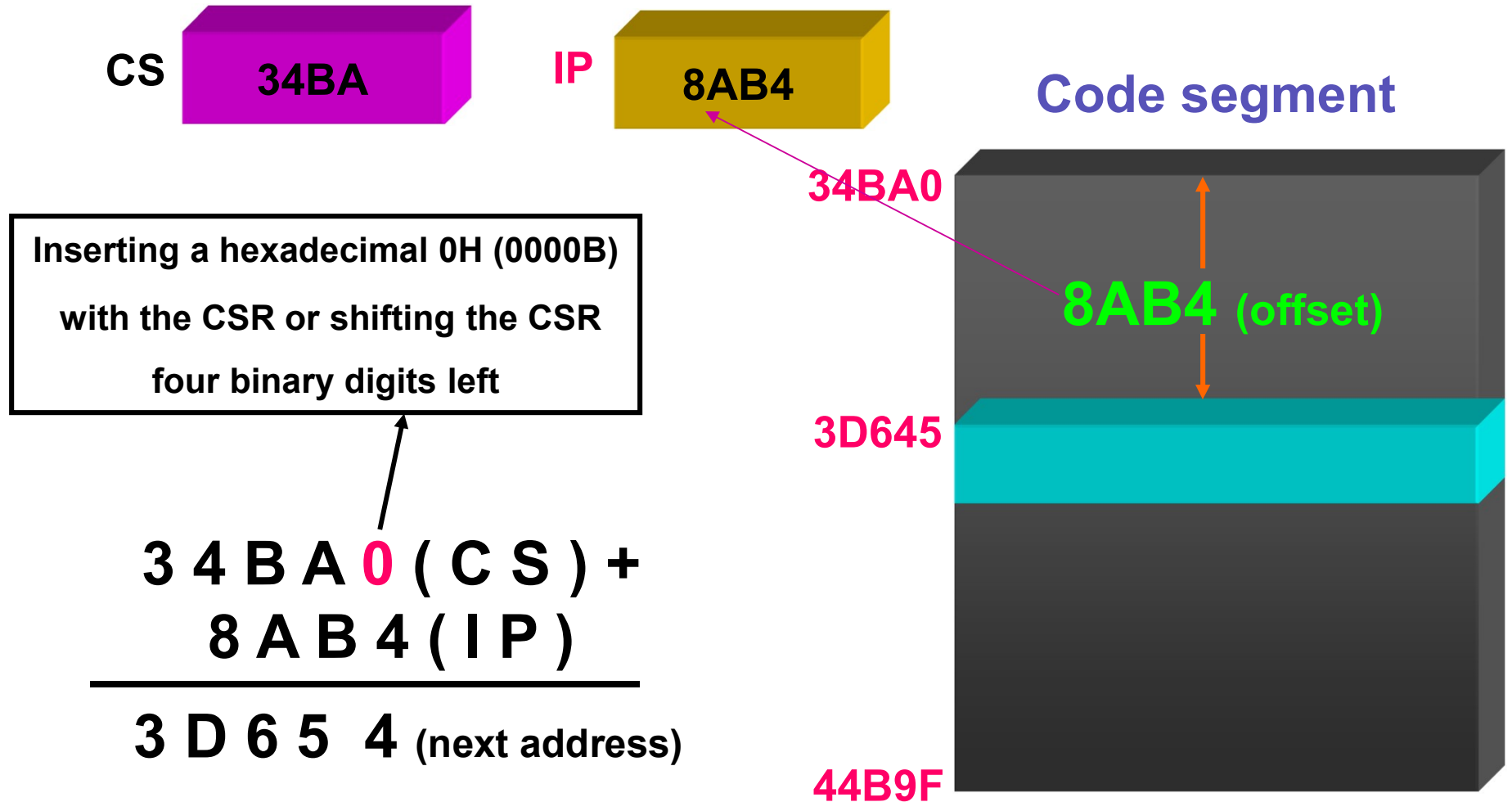
Instruction pointer and Code Segment

- The instruction pointer register contains a 16-bit offset address of instruction that is to be executed next.
- Instruction pointer values get incremented automatically after every instruction is executed.
- The value contained in the instruction pointer is called as an offset because this value must be added to the base address of the code segment, which is available in the CS register to find the 20-bit physical address.
- To form a 20-bit address of the next instruction, the 16 bit address of the IP is added (by the address summing block) to the address contained in the CS , which has been shifted four bits to the left.

Address Summing Block



CS:IP Scheme Example
(not required in the exam)



EXECUTION UNIT

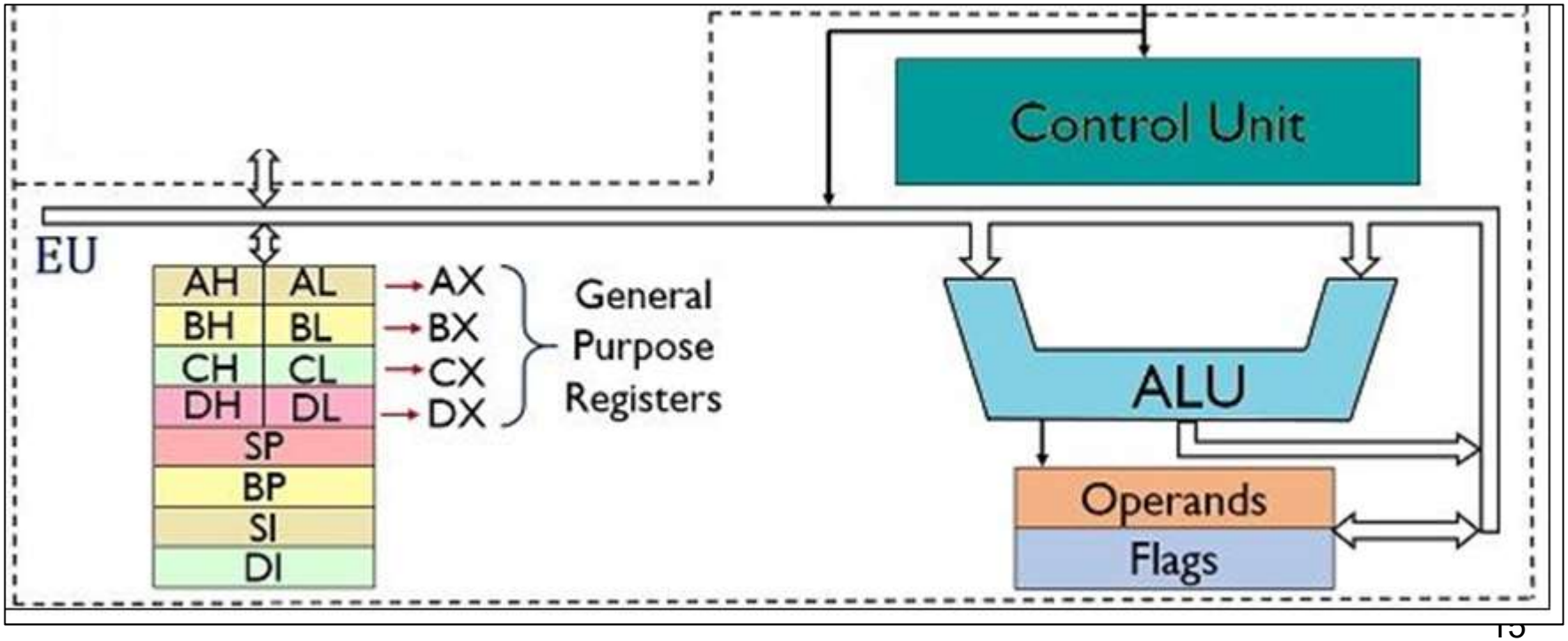
The EU performs below operations:

- Decodes instructions fetched by the BIU
- Generate control signals for data flow,
- Executes Arithmetic/Logic instructions.

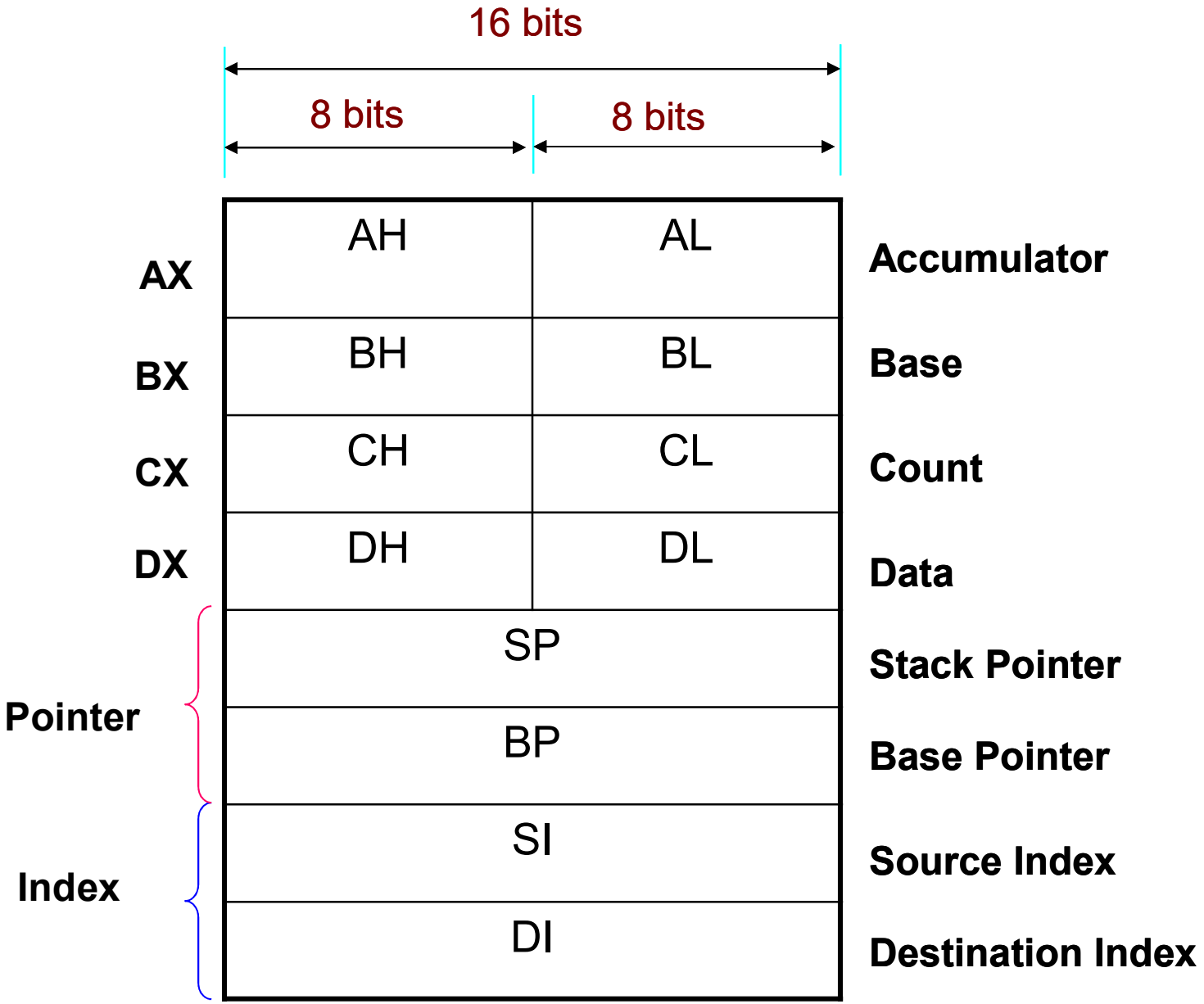
EXECUTION UNIT

The main parts are:

- **Control Unit (Instruction decoder and Control Circuit)**
- **General Purpose Registers**
- **Arithmetic and Logic Unit (ALU)**



EXECUTION UNIT – General Purpose Registers

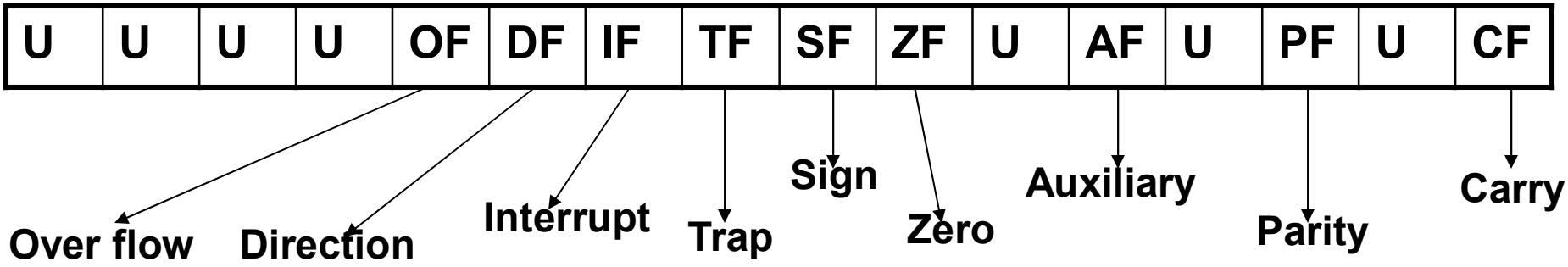


EXECUTION UNIT – General Purpose Registers

Register	Purpose
AX	**Accumulator register:** It gets used in arithmetic, logic and data transfer instructions.
BX	**Base register:** is used to hold the address of a procedure or variable.
CX	**Count register:** used as loop counter in string manipulation
DX	**Data regist**er: is used in multiplication and division.

Flag Register

- A flag is a flip flop which indicates some conditions produced by the execution of an instruction or controls certain operations of the EU .



U - Unused

Important Flags

Important Flags	Purpose
Carry (CF)	Holds the carry after addition or the borrow after subtraction
Parity (PF)	PF=0;odd parity, PF=1;even parity.
Zero (ZF)	Shows the result of the arithmetic or logic operation. Z=1; result is zero. Z=0; The result is non zero
Sign (SF)	Holds the sign of the result after an arithmetic/logic instruction execution. Sign Flag is set to 1 when result is negative. When result is positive it is set to 0.
Interrupt (IF)	Controls the operation of the INTR (interrupt request) I=0; INTR pin disabled. I=1; INTR pin enabled.

Lecture 02: CPU
PART2- Intel 80386

NEW 80386 Features

- First 32-bit microprocessor in the x86 family released in 1986.
- It contains 32-bit ALU, 32-bit Registers, 32-bit Data Bus, and 32-bit Address Bus
- Since it can address up to 2^{32} memeory locations then we can write:

$2^{32} = 2^2 * 2^{10} * 2^{10} * 2^{10} = 4 * 1K * 1K * 1K = 4$ GB

- So maximum physical memory of 80386 is 4 GB.
- It has a built-in Memory Management Unit to support Segmentation, Paging and Virtual Memory.

80386 Mode

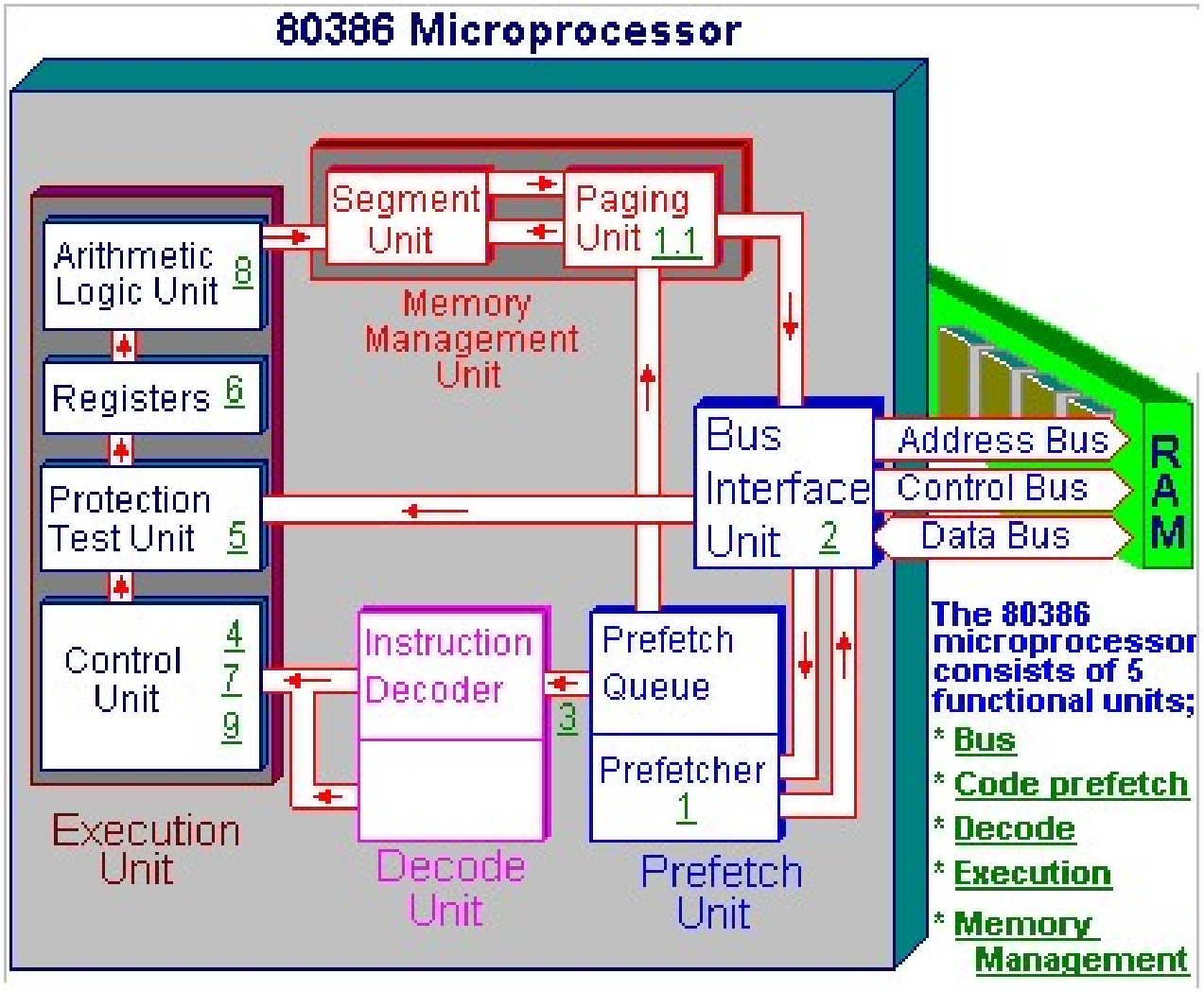
- Three Modes of Operation:
  - **Real Mode**: This is the Start-up mode. In this mode it behaves like a 8086, can access only 1 Mb memory, does not support multitasking/privilege levels/virtual memory/paging.
  - **Protected Mode**: In this mode, it can access all 4 Gb memory, supports multitasking/privilege levels/virtual memory/paging.

  To enable this mode, PE flag is set to 1, else system is in real mode
  - **Virtual 86 Mode**: This is a submode under Protected mode. In this mode, it provides virtual 1 Mb DOS Environment for DOS programs to work under multitask OS.

80386 Architecture

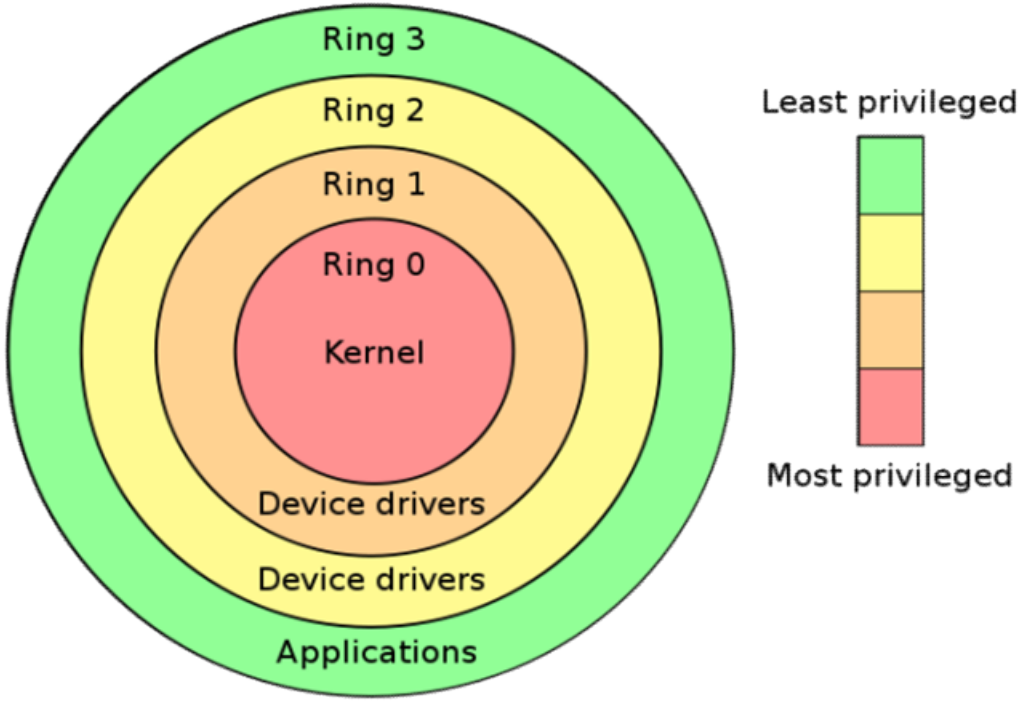
- 80386 has 5 functional units:
  1. Bus Interface unit
  2. Prefetch unit
  3. Decode unit
  4. Memory Management Unit:
     - Segmentation unit
     - Paging unit
  5. Execution unit

80386 Architecture Diagram (not required in the exam)



80386 Privilege levels

- Privilege levels determine what rights the code being executed has when issuing instructions, or accessing I/O ports and memory addresses. There are 4 privilege levels for 80386 processor architecture, and these are called rings. The four rings (0 to 3) are designed to protect the hardware resources, keeping user applications at level 3 (the least privilege) and the operating system kernel at ring 0 (the most privileged).



Kernel Mode vs User Mode in 80386

- **Kernel Mode**: the executing code has complete and unrestricted access to the underlying hardware. It can execute any CPU instruction and reference any memory address. Kernel mode is generally reserved for the lowest-level, most trusted functions of the operating system. Crashes in kernel mode are requires to restart the entire PC.
- **User Mode**: the executing code has no ability to directly access hardware or reference memory. Code running in user mode must delegate to Operating System to access hardware or memory. Due to the protection afforded by this sort of isolation, crashes in user mode are always recoverable. Most of the code running on your computer will execute in user mode.

Lecture 02: CPU
PART3- Intel CPU Evolutions

PC CPU Evolution

Since the first PC is introduced, CPU evolution has concentrated on five main areas:

- Increasing the clock cycling speeds
- Increasing the size of internal registers (bits)
- Adding and increasing the size of cache RAM
- Increasing the number of cores in a single chip

CPUs History

CPU	Year	Bus width	Freq.	Description
4004	1971	4	750 kHz	First Intel microprocessor.
8085	1976	8	3 MHz	Enhanced version of Intel 8-bit CPU.
8086/8088	1978	16	5-10 MHz	First generation of Intel x86 processors. Used in IBM PC
80386	1985	32	16-33 MHz	Third generation of x86 processors: First 32 bit architecture, with new processor modes.
Pentium	1993	32	60 - 66 MHz	Fifth generation of x86 processors: superscalar architecture, MMX. Intel shifts from numbers to names for its chips after the company learns it's impossible to trademark a number
Celeron	1998	32	366 - 400 MHz	Low-cost version of Pentium series.

CPUs History

CPU	Year	Bus width	Freq.	Description
Itanium	2001	64	733 - 800 MHz	High-performance 64-bit microprocessor.
Xeon	1998	32, 64	0.4 - 4.80 GHz	High-performance version of Pentium 4 CPU.
Core 2	2006	64	1.86 GHz	64-bit microprocessor. For normal desktop
Atom	2008	32, 64	600 - 800 MHz	Ultra-low power microprocessor.

CPUs History

CPU	Year	Bus width	Freq.	Description
Core i7	2008	64		• The higher the number, the more powerful the CPU • More powerful CPUs have more cores and are clocked at a faster frequency. • They all use the same sockets and motherboards • more powerful CPUs tend to have better support for higher RAM sizes and frequencies as well as higher overclocking speeds
Core i5	2009	64		
Core i3	2010	64		
Core i9	2017	64		

Modern Intel CPU Naming

U: Ultra-Low Power. The U rating is only for laptop processors. These draw less power and are better for the battery life

Example:- i7 7500u, i5 8250u, etc

Y: Low Power. Typically found on older generation laptops and mobile processors.

Example:- m3 8100Y, i5 8200Y, i7 8500Y etc.

T: Power Optimized for desktop processors.

Example:- i5 7500T, i5 7400T, i3 7300T, i3 7100T etc.

Q: Quad-Core. The Q rating is only for processors with four physical cores.

Example:- i7 7700HQ, i5 7300HQ etc.

H: High-Performance Graphics. The chipset has one of Intel's better graphics units

Example:- i7 7700HQ, i5 7300HQ, i7 8750H etc.

G: Includes Discrete Graphics. Typically found on laptops, this means there is a dedicated GPU with the processor.

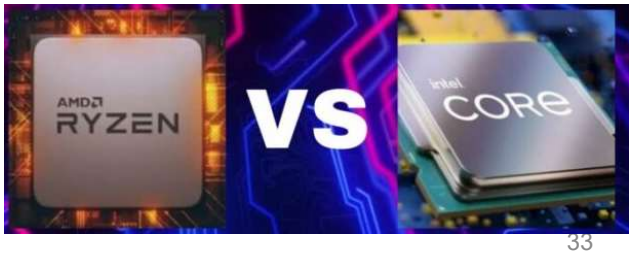
Example:- i7 8705G, etc.

K: Unlocked. This means you can overclock the processor above its rating.

Example:- i7 7700k, i7 8700k, i9 9900k, etc

AMD CPU vs Intel CPU

- AMD (Advanced Micro Devices) is a multinational semiconductor firm in the United States that develops and manufactures computer processors, graphics cards, and other hardware components. AMD, the world's second-largest chip maker behind Intel, is known for producing high-performance CPUs and GPUs at a cheaper cost.
- The primary distinction between Intel and AMD processors is their architecture:
  - Intel processors are noted for their single-threaded performance and faster clock speeds.
  - AMD processors, on the other hand, have more cores and threads, making them more suited for multithreaded applications like content production and video editing.



AMD vs Intel Samples
(not required in the exam)

	Model	Boost Clock	Cores/Threads	Price
1.	*Intel i9-12900K*	5.2 GHz	16/24	$599
2.	*AMD Ryzen 5950X*	4.9 GHz	16/32	$799
3.	*Intel i7-12700K*	5.0 GHz	12/20	$419
4.	*Intel i9-11900K*	5.3 GHz	10/16	$549
5.	*AMD Ryzen 5900X*	4.8 GHz	12/24	$549
6.	*AMD Ryzen 5800X*	4.7 GHz	8/16	$449
7.	*Intel i5-12600K*	4.9 GHz	10/16	$299
8.	*Intel i7-11700K*	5.0 GHz	8/16	$409